Amendment to the Claims:

This listing of claims will replace all prior versions and listings of claims in the application. Please enter new claims 31-38.

Listing of Claims:

1. (currently amended) A method comprising:

forming a thin film stack on a substrate, wherein the thin film stack includes at least a polysilicon layer and an oxide layer;

forming a hardmask layer on the thin film stack, wherein the hardmask layer is comprised of a carbon based material;

forming an anti-reflective coating (ARC) layer on the hardmask layer, wherein the ARC layer comprises a different material than the hardmask layer;

forming a resist layer on the ARC layer, wherein the resist layer is comprised of a carbon based material;

patterning the resist layer and the ARC layer;

etching the hardmask layer using the patterned ARC layer as a mask, wherein a portion of the resist layer is removed during the etching of the hardmask layer; and

etching the thin film stack using the hardmask layer as a mask.

2. (currently amended) The method of claim 1, wherein the ~~ARC layer is patterned with~~ resist layer is patterned using 193nm or less lithography.

3. (currently amended) The method of claim 2, wherein the thickness of the resist layer is less than 5000Å.

4. (original) The method of claim 3, wherein the hardmask has a thickness of between 1000 and 3000Å and the ARC layer has a thickness of between 100 and 500Å.

5. (original) The method of claim 3, wherein the hardmask layer comprises a material that has high selectivity to both polysilicon and oxide etch chemistries.

6. (original) The method of claim 3, wherein the hardmask layer comprises amorphous carbon.

7. (original) The method of claim 6, wherein the hardmask layer comprises Applied Materials® Advanced Patterning Film™ (APF™).

8. (original) The method of claim 3, wherein the ARC layer is removed during the etching of the thin film stack.

9. (currently amended) The method of claim 3, further comprising removing the hardmask layer ~~material~~ from the thin film stack.

10. (currently amended) A method comprising:

forming a flash memory gate stack on a substrate;

forming a hardmask layer on the flash memory gate stack wherein the hardmask layer is comprised of a carbon based material;

forming an anti-reflective coating (ARC) layer on the hardmask layer, wherein the ARC layer comprises a different material than the hardmask layer;

forming a resist layer on the ARC layer, wherein the resist layer is comprised of a carbon based material;

patterning the resist layer and the ARC layer;

etching the hardmask layer using the patterned ARC layer as a mask, wherein a portion of the resist layer is removed during the etching of the hardmask layer; and

etching the flash memory gate stack using the hardmask layer as a mask.

11. (currently amended) The method of claim 10, wherein the ~~ARC layer is patterned with~~ resist layer is patterned using 193nm or less lithography.

12. (currently amended) The method of claim 11, wherein the thickness of the resist layer is less than 5000Å.

13. (original) The method of claim 12, wherein the flash memory gate stack is comprised of a gate dielectric layer, a floating gate layer, an inter-electrode dielectric layer, and a control gate electrode layer.

14. (original) The method of claim 12, wherein the hardmask has a thickness of between 1000 and 3000Å and the ARC layer has a thickness of between 100 and 500Å.

15. (original) The method of claim 12, wherein the hardmask layer comprises a material that has high selectivity to both polysilicon and oxide etch chemistries.

16. (original) The method of claim 12, wherein the hardmask layer comprises amorphous carbon.

17. (original) The method of claim 16, wherein the hardmask layer comprises Applied Materials® Advanced Patterning Film™ (APF™).

18. (original) The method of claim 12, wherein the ARC layer is removed during the etching of the flash memory gate stack.

19. (currently amended) The method of claim 12, further comprising removing the hardmask layer ~~material~~ from the flash memory gate stack.

20. – 30. (canceled)

31. (new) A method comprising:

forming a first dielectric layer on a substrate;

forming a thin film stack above said first dielectric layer, wherein said thin film stack comprises a second dielectric layer between two polysilicon layers;

forming a hardmask layer on said thin film stack;

forming an anti-reflective coating (ARC) layer on said hardmask layer, wherein said ARC layer comprises a different material than said hardmask layer;

patterning said ARC layer to form a patterned ARC layer;

etching said hardmask layer using said patterned ARC layer as a mask; and

etching said thin film stack using said hardmask layer as a mask, wherein said patterned ARC layer is completely removed during the etching of said second dielectric layer between the two polysilicon layers of said thin film stack.

32. (new) The method of claim 31, wherein said ARC layer is patterned with a resist layer using 193nm or less lithography.

33. (new) The method of claim 32, wherein the thickness of said resist layer is less than 5000Å.

34. (new) The method of claim 33, wherein said hardmask has a thickness of between 1000 and 3000Å and said ARC layer has a thickness of between 100 and 500Å.

35. (new) The method of claim 33, wherein said hardmask layer comprises a material that has high selectivity to both polysilicon and dielectric etch chemistries.

36. (new) The method of claim 33, wherein said hardmask layer comprises amorphous carbon.

37. (new) The method of claim 36, wherein said hardmask layer comprises Applied Materials® Advanced Patterning Film™ (APF™).

38. (new) The method of claim 33, further comprising removing said hardmask layer from said thin film stack.